1765

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ko et al.

Serial No.: 09/711,324

Filed: November 13, 2000

For: ETCHANT WITH SELECTIVITY FOR DOPED SILICON DIOXIDE OVER UNDOPED SILICON DIOXIDE AND SILICON NITRIDE, PROCESSES WHICH EMPLOY THE ETCHANT, AND STRUCTURES FORMED THEREBY

Confirmation No.: 7008

Examiner: K. Chen

Group Art Unit: 1765

Attorney Docket No.: 2269-3526.4US
(97-1136.05/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

June 26, 2003
Date

Signature

Deidra J. Pfeil
Name (Type Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

U.S. Patent No.	Publication Date	Patentee
4,529,476	07/1985	Kawamoto et al.
6,018,184	01/2000	Becker
6,066,555	05/2000	Nulty et al.
6,110,831	08/2000	Cargo et al.
6,117,791	09/2000	Ko et al.
6,277,720 B1	08/2001	Doshi et al.
6,303,496 B1	10/2001	Yu
6,483,172 B1	11/2002	Cote et al.

Foreign Patent Documents

Document No.	Publication Date	Patentee
61251138	08/1986	JP
0721205 A2	07/1996	EPO
WO 98/49719	11/1998	PCT

Other Documents

Wolf, S., et al., Silicon Processing for the VLSI Era, Vol. 1, Process Technology, Lattice Press, 1986, pp. 520-523.

Williams, K., BSAC Etch Rates for Micromachining and IC Processing, U.C. Berkeley Microfabrication Lab., Berkeley Sensor & Actuator Center, http://www-bsac.eecs.berkeley, edu/db/etchrates.html.

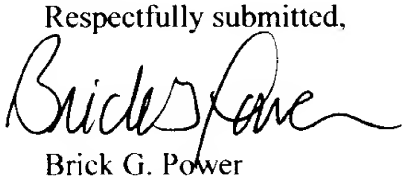
Williams, K., VLSI Etchants, Chapter 1.5, Rev. 11/97, http://microlab.berkeley,edu/labmanual/chap1/1.5.html.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,



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Date: June 26, 2003
BGP/ps:djp

Enclosures: Form PTO-1449
Copy of documents cited
Check No. 4569 in the amount of $180.00

Document in ProLaw

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
3526.4US (97-1136.05/US)	**09/711,324**
Applicant **Ko et al.**	
Filing Date **November13, 2000**	Group Art Unit **1765**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,529,476	07/1985	Kawamoto et al.			
	6,018,184	01/2000	Becker			
	6,066,555	05/2000	Nulty et al.			
	6,110,831	08/2000	Cargo et al.			
	6,117,791	09/2000	Ko et al.			
	6,277,720 B1	08/2001	Doshi et al.			
	6,303,496 B1	10/2001	Yu			
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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
	61251138	08/1986	JP			X	
	0721205 A2	07/1996	EPO				
	WO 98/49719	11/1998	PCT				

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		Wolf, S., et al., Silicon Processing for the VLSI Era, Vol. 1, Process Technology, Lattice Press, 1986, pp. 520-523.
		Williams, K., BSAC Etch Rates for Micromachining and IC Processing, U.C. Berkeley Microfabrication Lab., Berkeley Sensor & Actuator Center, http://www-bsac.eecs.berkeley.edu/db/etchrates.html.
		Williams, K., VLSI Etchants, Chapter 1.5, Rev. 11/97, http://microlab.berkeley.edu/labmanual/chap1/1.5.html.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.